CLAIMS

1. A pulse detector comprising: input means for inputting an input signal pulse; leading edge detector means connected to the input means for detecting a leading edge of a first input signal pulse; trailing edge detector means connected to the input means for detecting a wailing edge of the first input signal pulse; first timing means, clocked by a clock signal, connected to the leading edge detector means and to the trailing edge detector means for determining a pulse duration time between detection of the leading edge and detection of the trailing edge; divisor means connected to the timing means for dividing the pulse duration time to produce a divided pulse duration time; second timing means connected to the divisor means for outputting a pulse narrower than the input signal pulse the divided pulse duration time after detection of the leading edge of a second input pulse representative of a mid-point of the second input signal pulse; and combining means connected to the second timing means and to the input means for combining the pulse narrower than the input signal pulse with the clock signal to provide an output pulse in synchronisation with the midpoint of the second input signal pulse.

2. A pulse detector as claimed in claim 1, further comprising pulse inverting means connected to the input means for inverting at least two successive signal pulses to provide an output pulse corresponding to a mid-point of a trough between at least two successive signal pulses.

3. A pulse detector as claimed in claim 2, comprising first leading edge detector means connected to the input means; first trailing edge detector means connected to the input means; first timing means connected to the first leading edge detector means and to the first trailing edge detector means for determining a first pulse duration time between detection of the leading edge and detection of the trailing edge of the signal pulse; and first divisor means connected to the first timing means for dividing the first pulse duration time for producing a first divided pulse duration time; second timing means connected to the divisor means for outputting a pulse narrower than the input signal pulse the divided pulse duration time after detection of the leading edge of a second input pulse representative of a mid-point of the second input signal pulse; and combining means connected to the second timing means and to the clock signal for combining the pulse narrower than the input signal pulse with the clock signal to provide an output pulse in synchronisation with the midpoint of the second input signal pulse; and second leading edge detector means connected to the pulse inverter means; second trailing edge detector means

connected to the inverter means; third timing means connected to the second leading edge detector means and to the second trailing edge detector means for determining a second pulse duration time between detection of the leading edge and detection of the trailing edge of the inverted signal pulse; and second divisor means connected to the third timing means for dividing the second pulse duration time to produce a second divided pulse duration time; fourth timing means connected to the divisor means for outputting a pulse narrower than the inverted signal pulse the second divided pulse duration time after detection of the leading edge of a second inverted pulse representative of a mid-point of the second. inverted signal pulse; and combining means connected to the fourth timing means and to the clock signal for combining the pulse narrower than the input signal pulse with the clock signal to provide an output pulse in synchronisation with the midpoint of a trough between the at least two signal pulses.

4. A pulse detector as claimed in claim 1, wherein the timing means comprises count-up means for producing a first count representative of the pulse duration time; the leading edged detector means and the trailing edge detector means comprise an enable port of the count-up means; the divisor means comprises arithmetic divider means for receiving a first count from the count-up means, halving the first count to produce a second count equal to half the first count and for transferring the second count to count-down means initiatable by reception at an enable port thereof of a second input pulse such that on completion of counting down through the second count the count-down means outputs the pulse narrower than the input signal pulse representative of the mid-point of the second input signal pulse.

5. A pulse detector as claimed in claim 4, further comprising clock means connected to frequency multiplier means which is connected to the count-up means and the count-down means for synchronising the count-up means and the count-down means at a frequency higher than that of the clock means.

6. A pulse detector as claimed in claim 1 wherein the input means comprises switch means for switching input between the clock means and a data input port.

7. A pulse detector as claimed in claims 4 to 6, wherein the combining means is an AND gate electrically connected to the clock signal and to the count-down means for combining the clock signal with the pulse narrower than the input signal pulse output by the count-down means.

8. A pulse detector as claimed in claim 7, wherein buffer amplifier means are provided between the input means and the count-up means and the count-down means for preventing

loading variations on the timing means and/or to match a first propagation time of the signal pulse through the switching means and buffer amplifier means with a second propagation time of the signal pulse through the count-up means, the count-down means and the divisor means.

9. A pulse detector as claimed in claim 3, further comprising peak and trough combination means for combining the first output pulse and the second output pulse.

10. A pulse detector as claimed in claim 9, wherein the peak and trough combination means is an EXOR gate.